DIGITAL CHIP FABRICATION

SILICON PROVEN LEAKY INTEGRATE & FIRE NEURON

TEAM: SDMAY23-28

CLIENT & ADVISOR: DR HENRY DUWE

Our Team

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EE

Team Management
System Organization
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Bring-up Plan

Tyler Green

CprE

Software Tools Environment
SNN Design / Implementation

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SNN Design / Implementation

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Software Tool Research
Caravel Tutorial Document

INTRODUCTION

Project Overview

Problem Description & Location

At ISU, it is rare to find undergraduate students in computer or electrical engineering that have created, fabricated, and brought-up a digital ASIC.

- Traditionally large barrier to entry

Client's Goals

Dr. Duwe is investigating opportunities for a co-curricular where students fabricate and physically implement digital chip designs.

Our Project Objectives

Design and silicon-prove an ASIC.

Compose a bring-up plan for our design.

Develop documentation for future students.

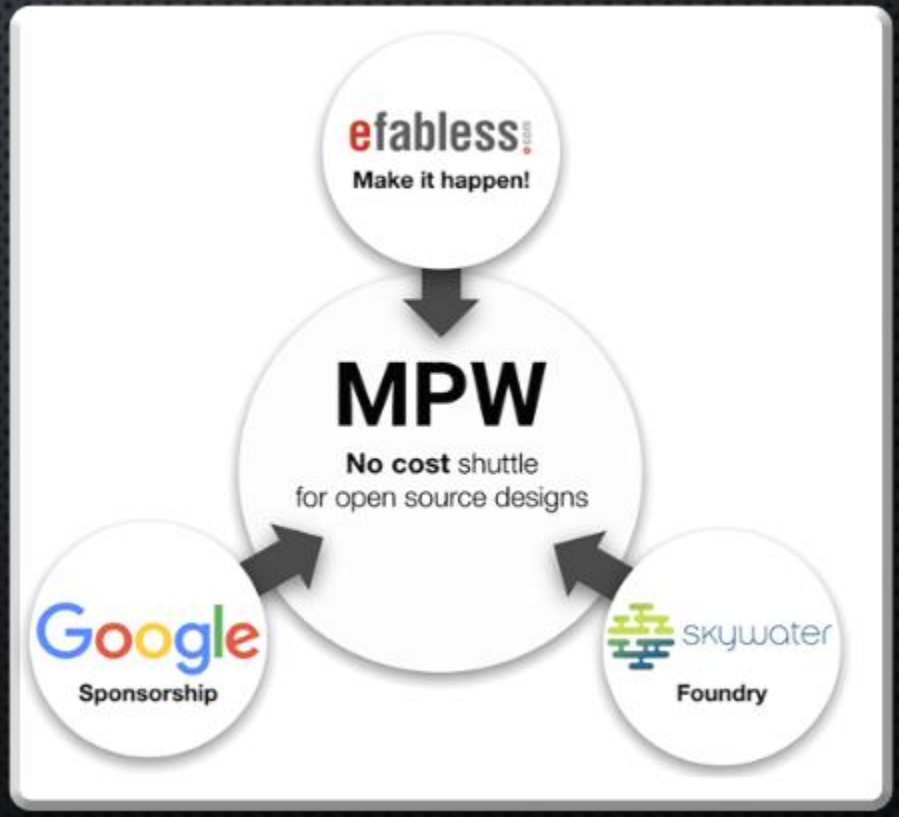
Background & Hardware

Manufacturing EFABLESS

- Doped Silicon Composes Transistors
- Transistors Compose Logic
- Efabless Organizes all the components

Process Design Kit SKYWATER

- Logic Combinations create Standard Cells
- Standard Cells are Spec-ed for Fabrication
- Specs Distributed as Process Design Kit (PDK)



https://efabless.com/open_shuttle_program

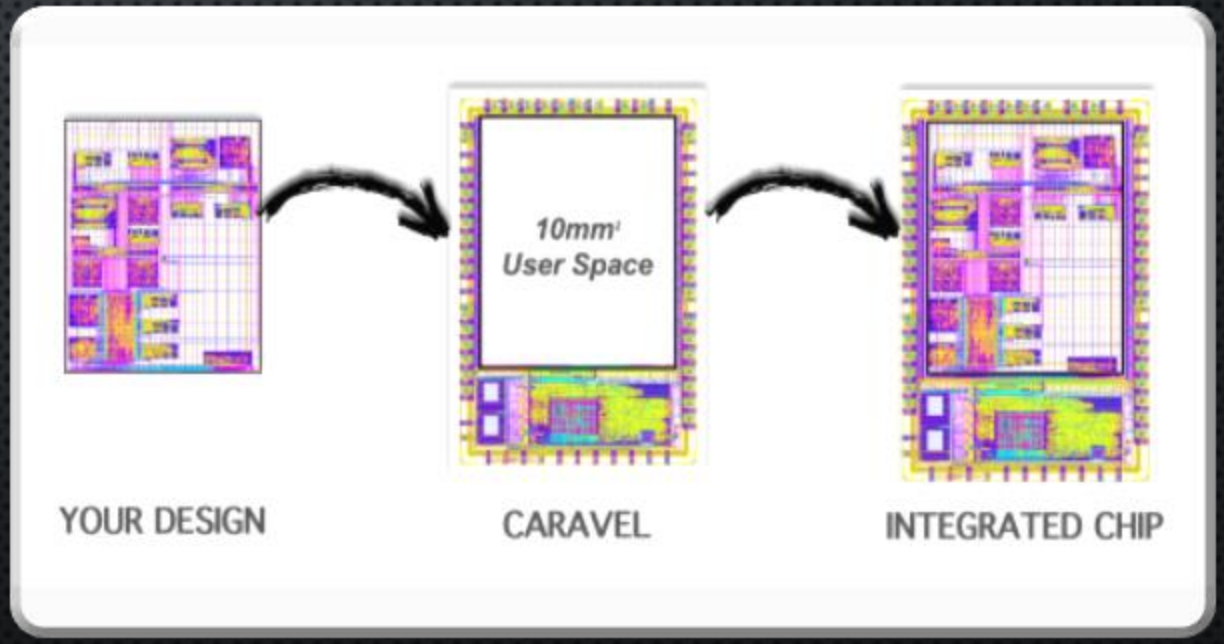
Background & Hardware

Hardware Description
CARAVEL HARNESS /USER AREA

- Verilog Defines User Functionality
- Wrapper to Standardize Designs

ASIC Flow OPENLANE

- Map Verilog to Netlist
- Place Cells, Connect Power/Clock
- Define Fabrication Masks



https://efabless.com/open_shuttle_program


ABOUT OUR PROJECT

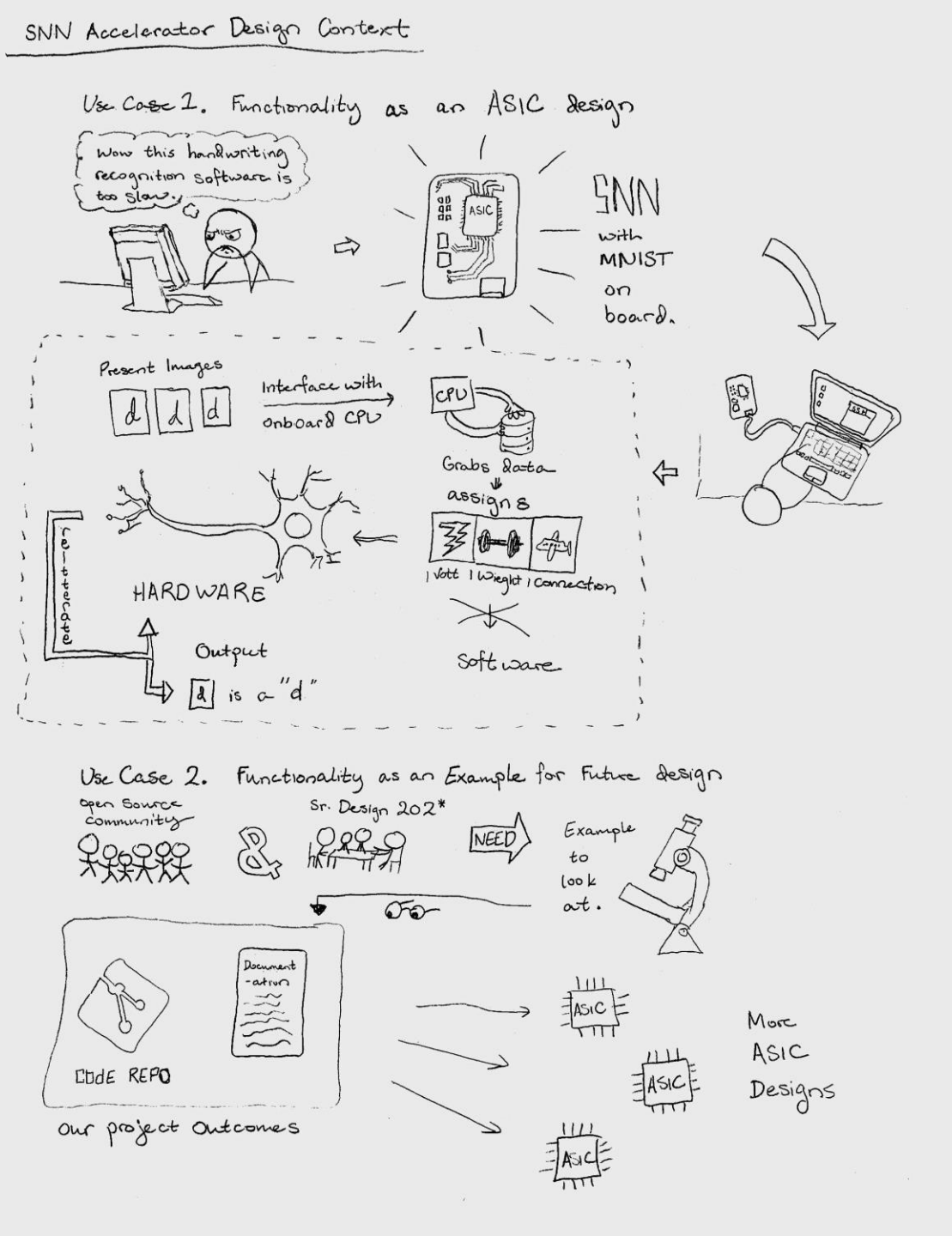
SNN Model Context

Machine Learning in Medical Imaging

- Identify diseases, injuries, tumors, etc…
- Speed up a lengthy process
- "ML (…) will have a greater influence in the future" [1]

The SNN

- "Bridge gap between Neuroscience and ML"[2]
- Closer to biology
- Typically, lower power
- Discrete electrical signals (digital)
- Accessible and scalable with MNIST data set



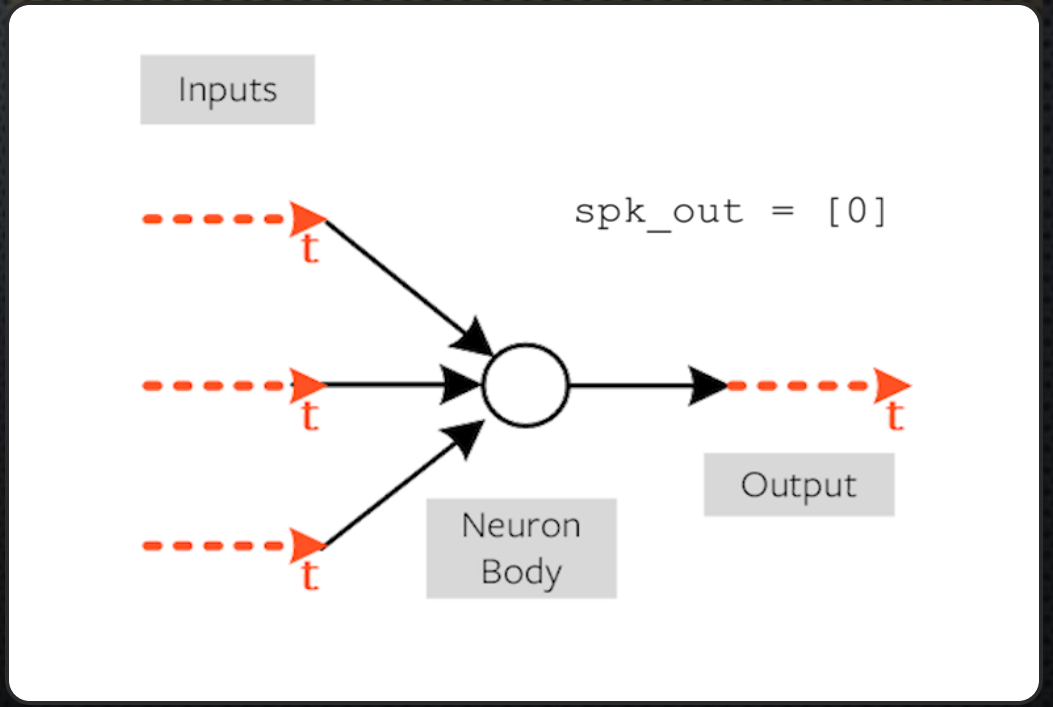
Spiking Neural Network Description

Neuron Model
Leaky Integrate and Fire

Network Model
snnTorch

- Allows easy network design and testing
- Allows us to export weights

snnTorch



"Training Spiking Neural Networks Using Lessons From Deep Learning", snntorch.readthedocs.io

Application

Classifying Handwritten Digits

MNIST Dataset

Training Set

60,000 images (28x28) - labels (0-9)

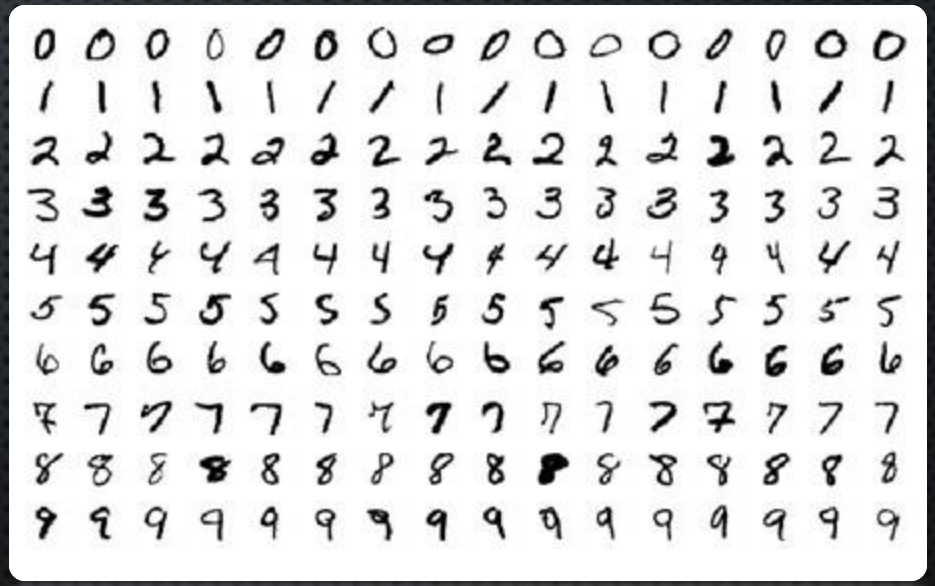
Testing Set

10,000 images

Reason for Using Handwritten Digits

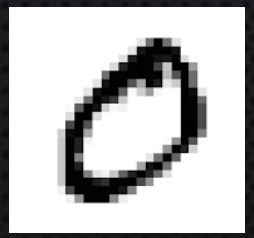
Simple application

Size constraints



https://www.researchgate.net/figure/A-sample-of-the-MNIST-handwritten-digits_fig3_339204564

Spiking Neural Network



Pixels

Rate coding

Spikes

0
1
2
3
4
5
6
7
8
9

Weights

10
3
1
1
4
0
3
7
4
6

Output Spikes


SYSTEM ARCHITECTURE

Design Overview

Generate

- Rate-encoded spikes
- Repeat for all pixels

Load Spikes/Weights

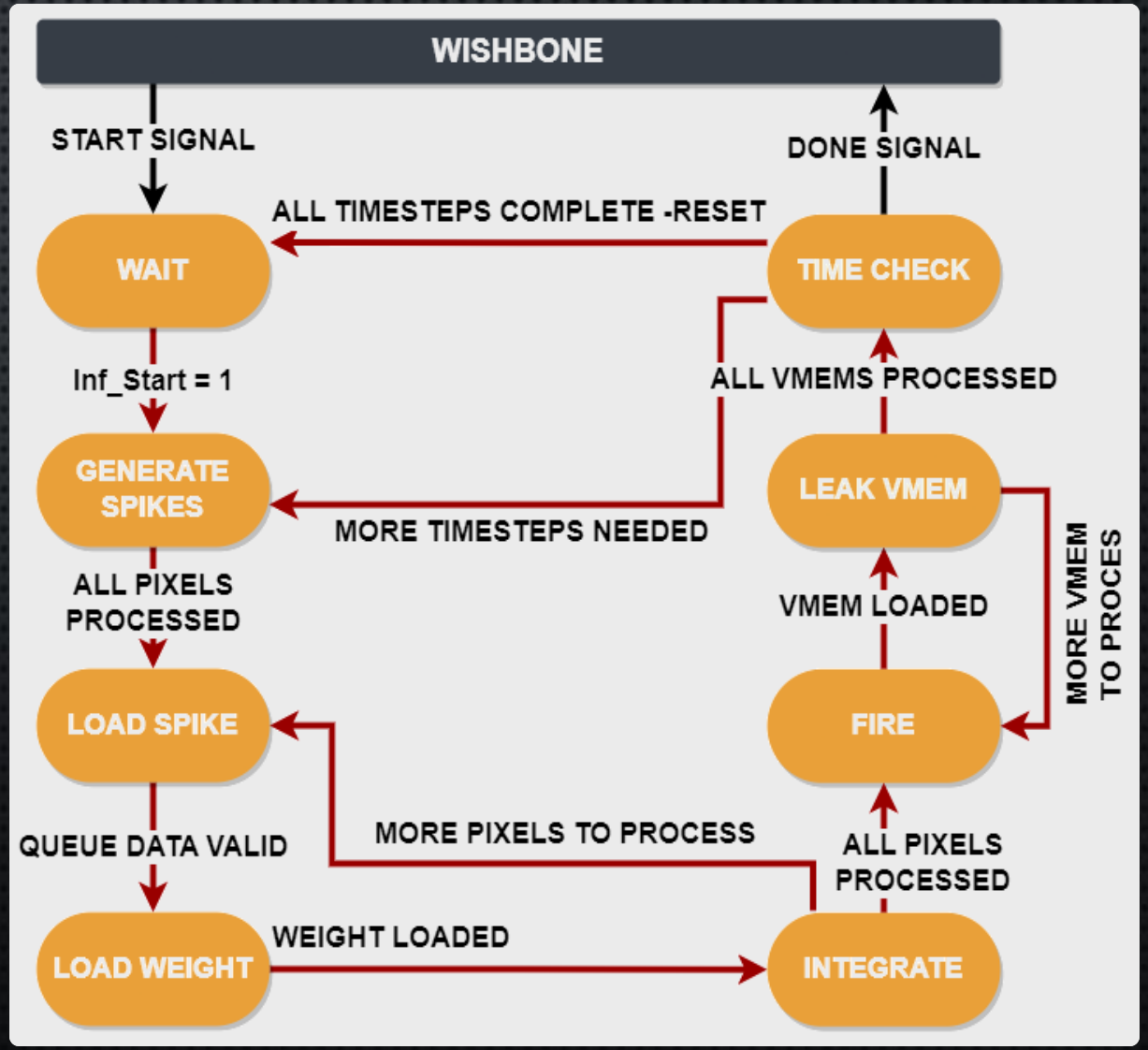
- Data movement States
- Send to and from Neuron Unit

Integrate/Leak/Fire

- Build up Membrane voltage
- Repeat for all pixels
- Leak each time step
- Fire according to Vmem at neuron ID
- Repeat for all Membrane Voltages

Wait/Time Check

- Controls Beginning and End of process
- Wait is default state



Data Path

Wishbone Feed

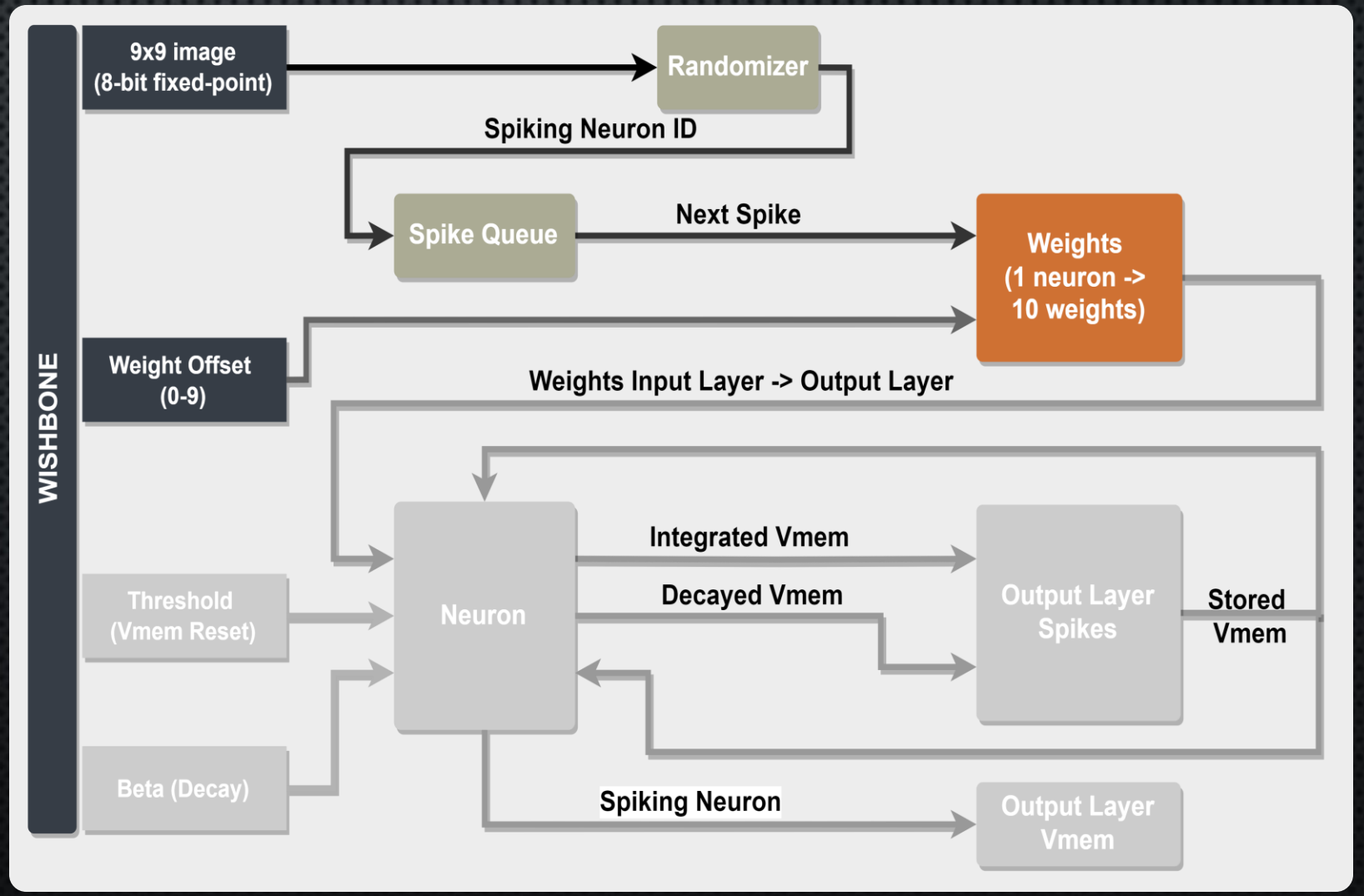
- Pixel values <- MNIST
- Weights <- pretrained snnTorch network
- Addresses <- CPU

Randomizer

- Pseudo random no. generator
- Seed with image values

Spike Queue

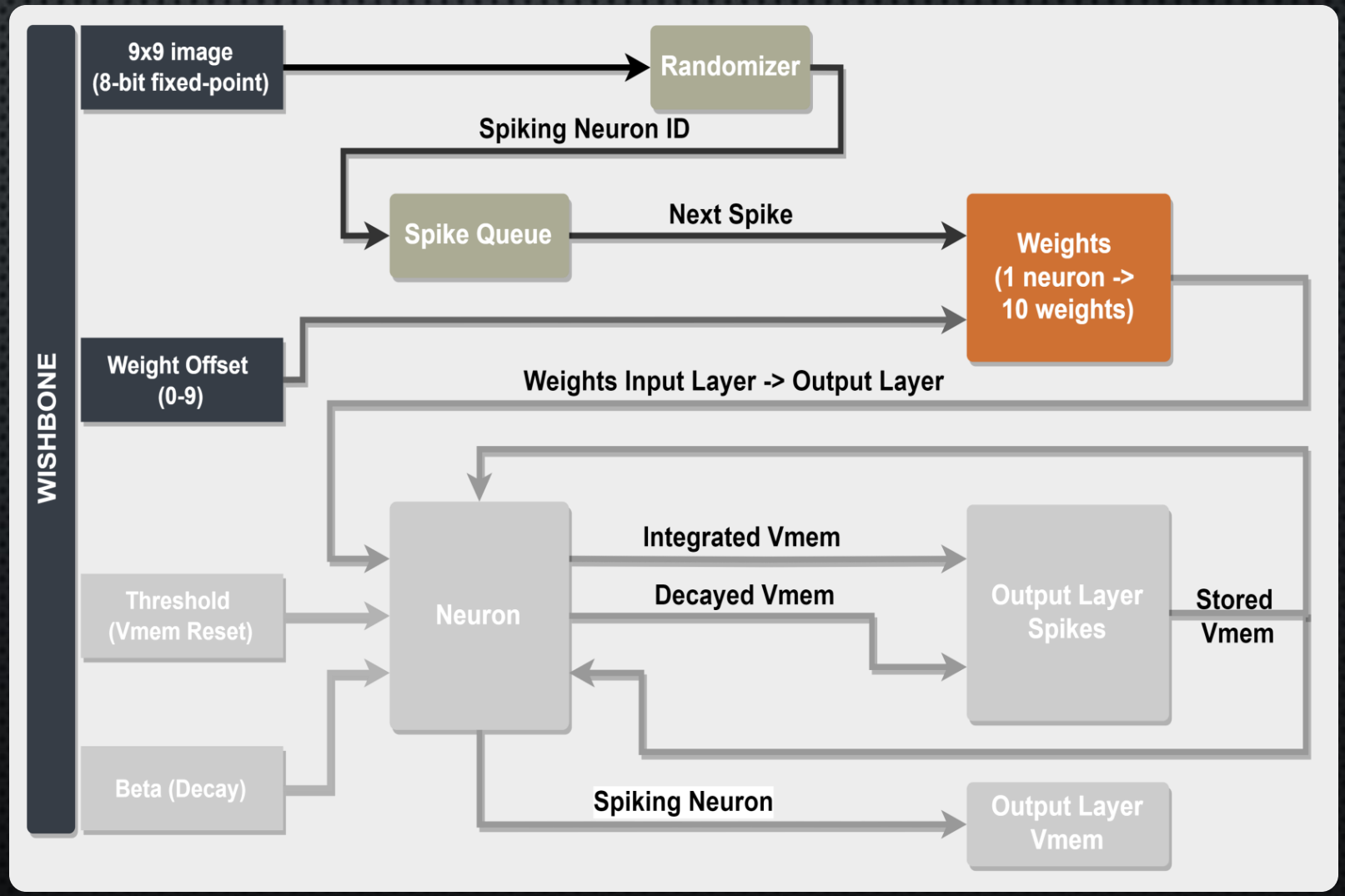
- FIFO holder for Spikes



Data Path

Neuron

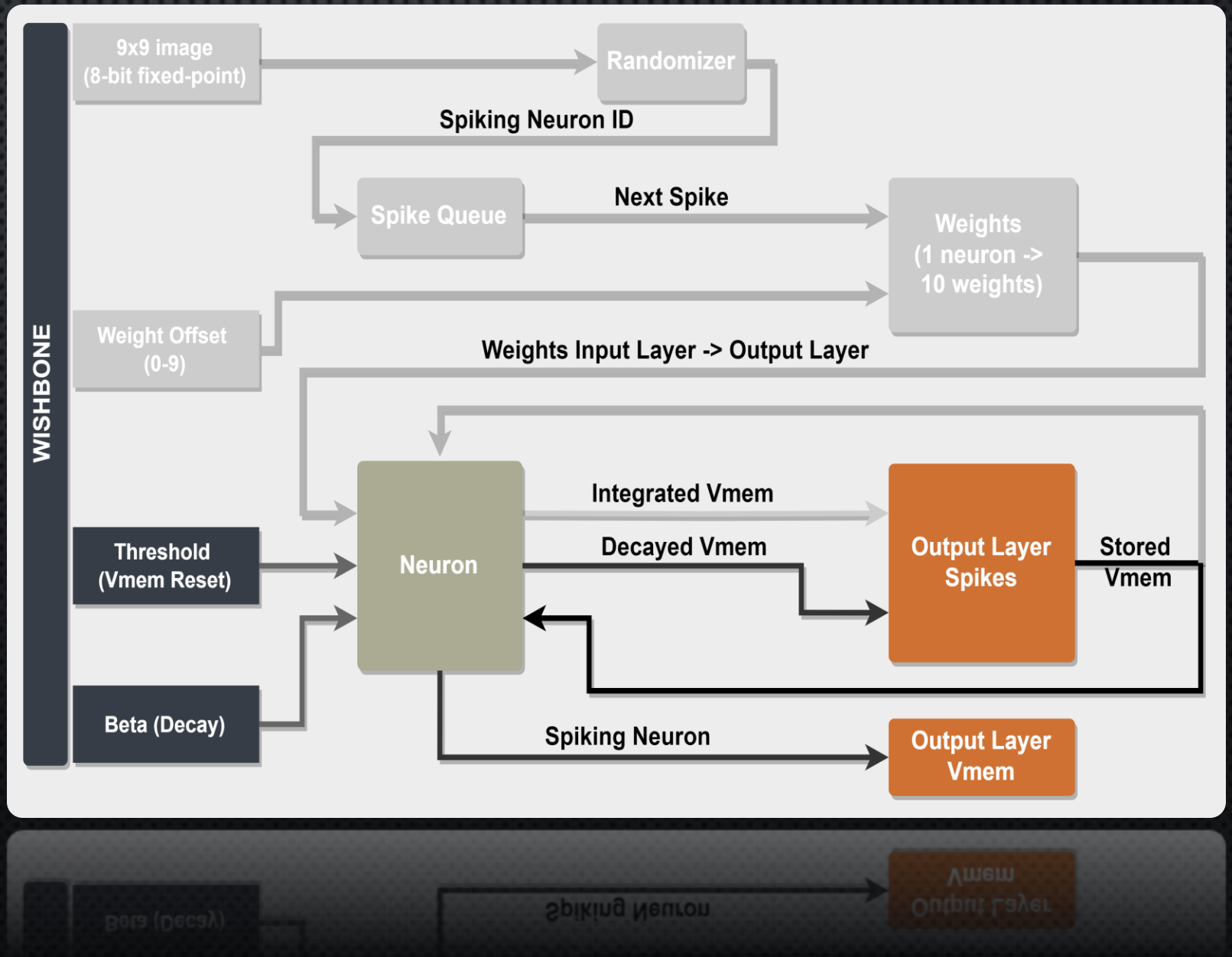
- LIF hardware model



Data Path

Neuron

- LIF hardware model



Neuron Unit

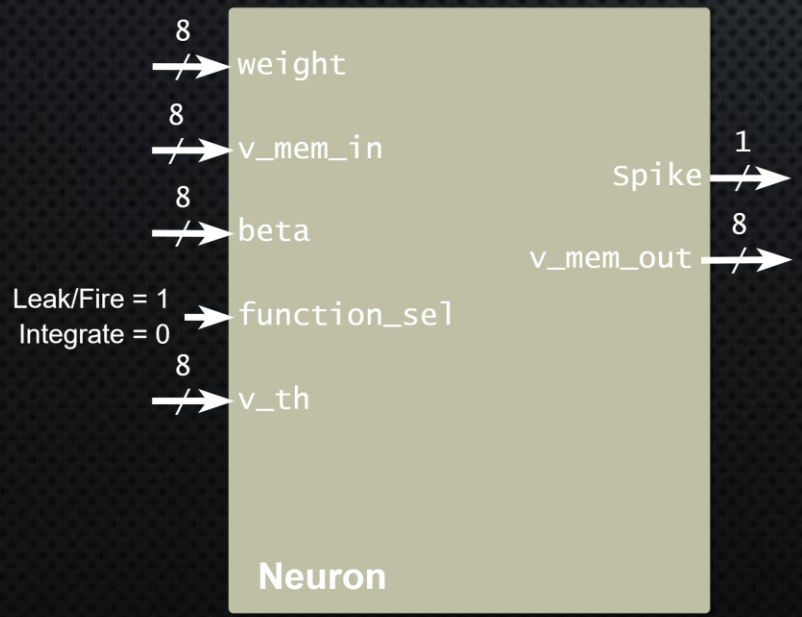
Equations Describing Neuron Behavior

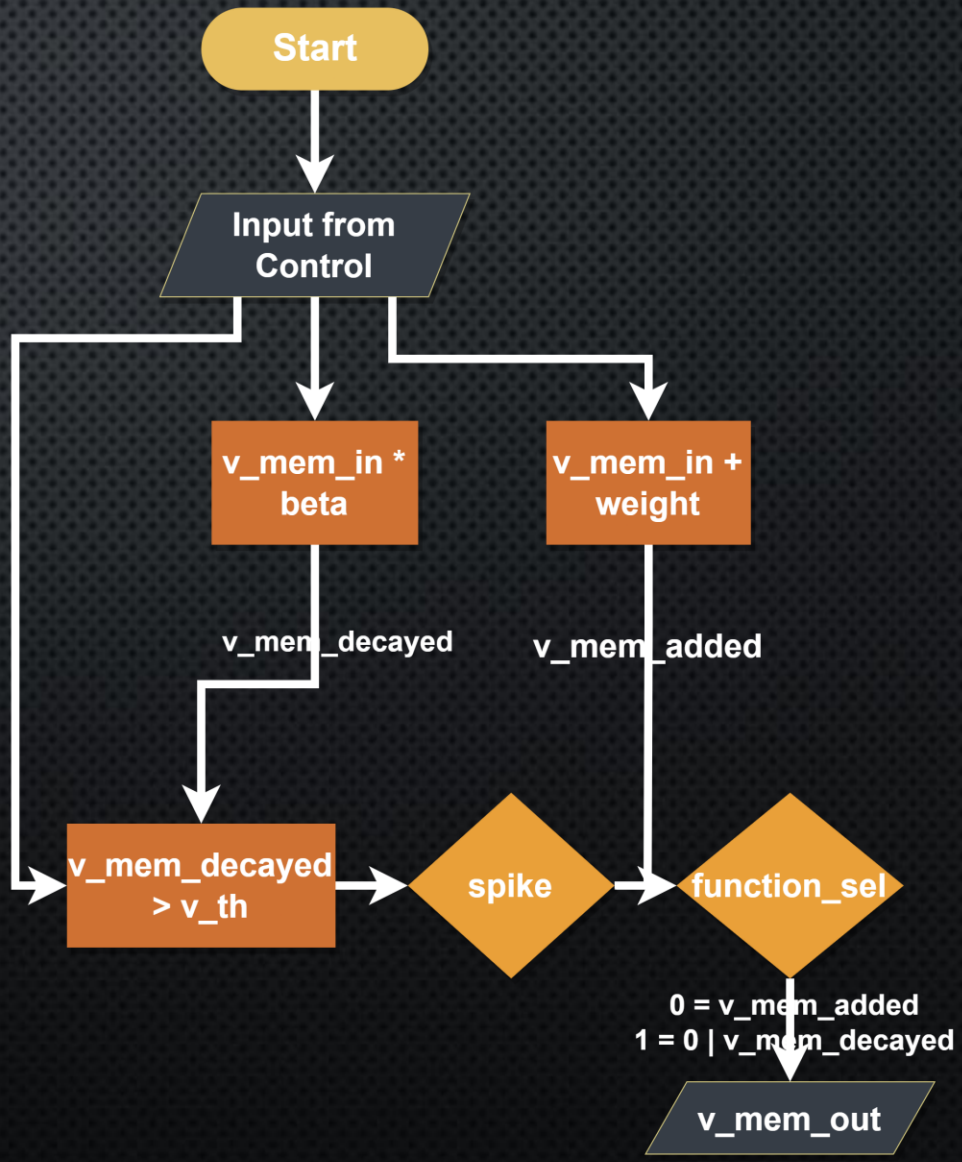
$U[T] > U_{thr} \Rightarrow S[T+1] = 1$

$U[t+1] = \beta U[t] + I_{in}[t+1] - RU_{thr}$

$U[t+1] = \beta U[t] + I_{syn}[t+1] - R(\beta U[t] + I_{in}[t+1])$

I/O Diagram





DESIGN OUTCOMES

Work Accomplishments

Goal 1 – SNN Submission

Client Request

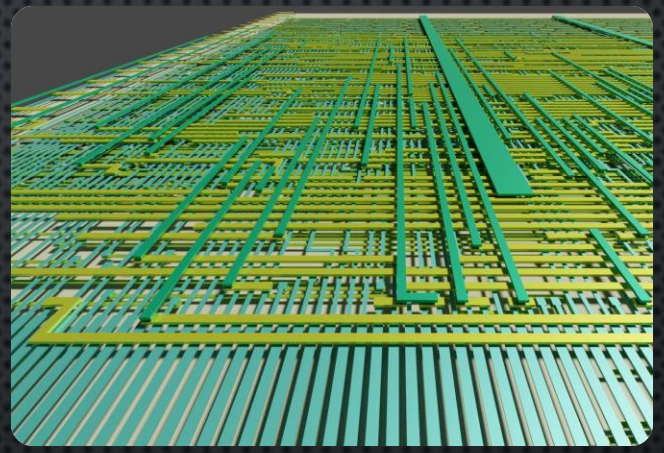
To silicon prove a chip design.

Product to be Delivered

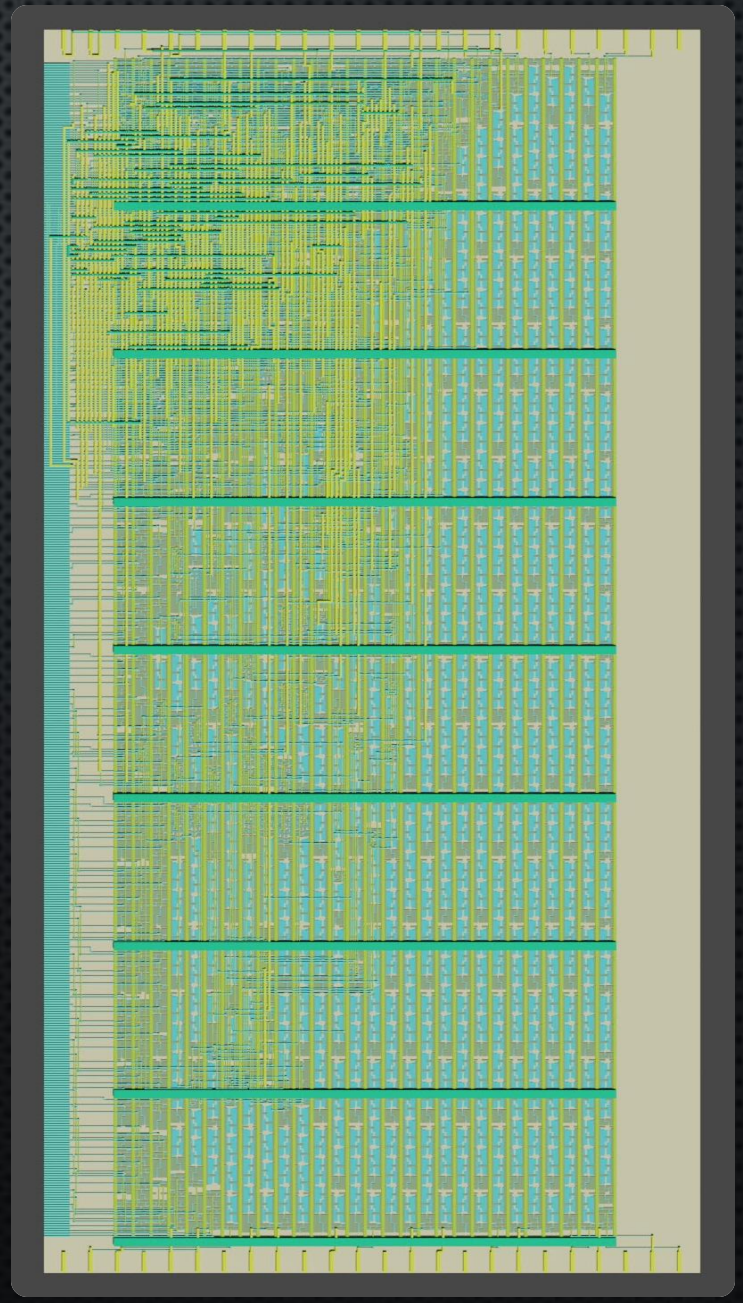
Silicon-proven neuron for a spiking neural network.

Contents of Product

Silicon-proven SNN neuron ready for fabrication.



```
No DRC Violations found
{{Klayout Pin Label Purposes Overlap
{{STEP UPDATE}} Executing Check 14 o
in CUSTOM klayout_gds_drc_check
run: klayout -b -r /home/tjgreen/mpw
_project_wrapper -rd report=/home/tj
/git/sdmay23-28/precheck_results/29_
29/logs/klayout_zeroarea_check.log
No DRC Violations found
{{Klayout ZeroArea CHECK PASSED}} Th
{{FINISH}} Executing Finished, the f
{{SUCCESS}} All Checks Passed !!!
Generating LALR tables
WARNING: 183 shift/reduce conflicts
05:54:22 Sat Apr 29 tjgreen@tg-arch
$
```



Renderings of the SNN Control Logic & Prechecks Passed ->

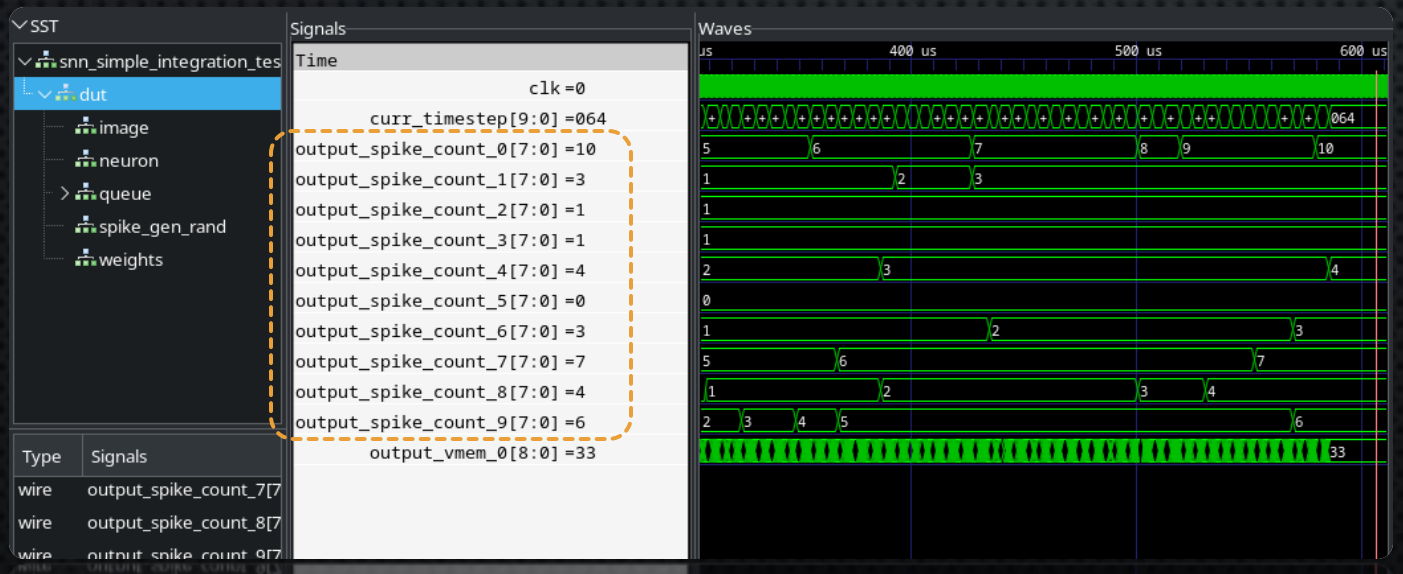
Goal 1 – Final Results

Simulation of Full Design

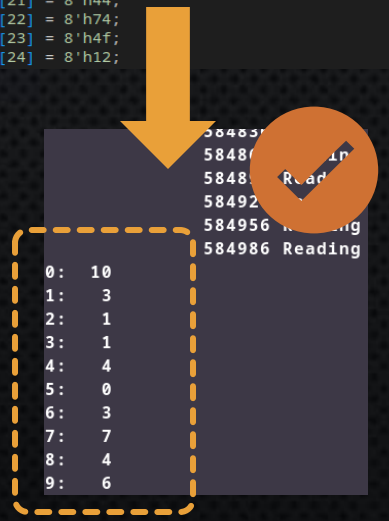
- 9 x 9 image
- Simulated as signals sent by CPU
- 83% snnTorch accuracy translates to 77% accuracy
  - Less precision (floating point to 8-bit fixed point)

https://python-course.eu/machine-learning/training-and-testing-with-mnist.php

```
integer i;

initial begin
    clock = 0;
    forever begin
    #5 clock = ~clock;
end end

initial
begin
    $dumpfile("snn_simple_integration_test.vcd");
    $dumpvars(0, snn_simple_integration_test_tb);

    // initialize image, this is a 0
    dut.image.mem[0] = 8'h00;
    dut.image.mem[1] = 8'h00;
    dut.image.mem[2] = 8'h00;
    dut.image.mem[3] = 8'h00;
    dut.image.mem[4] = 8'h01;
    dut.image.mem[5] = 8'h00;
    dut.image.mem[6] = 8'h00;
    dut.image.mem[7] = 8'h00;
    dut.image.mem[8] = 8'h00;
    dut.image.mem[9] = 8'h00;
    dut.image.mem[10] = 8'h00;
    dut.image.mem[11] = 8'h00;
    dut.image.mem[12] = 8'h08;
    dut.image.mem[13] = 8'h3e;
    dut.image.mem[14] = 8'h18;
    dut.image.mem[15] = 8'h00;
    dut.image.mem[16] = 8'h00;
    dut.image.mem[17] = 8'h00;
    dut.image.mem[18] = 8'h00;
    dut.image.mem[19] = 8'h00;
    dut.image.mem[20] = 8'h05;
    dut.image.mem[21] = 8'h44;
    dut.image.mem[22] = 8'h74;
    dut.image.mem[23] = 8'h4f;
    dut.image.mem[24] = 8'h12;
```



Waveform of Spikes Accumulating



Goal 2 - Bring Up Plan

Client Request:

Develop a bring up plan for future students to use to bring up our design on the Caravel Infrastructure.

Product to be Delivered:

Bring up plan for our chip design

Contents of Product:

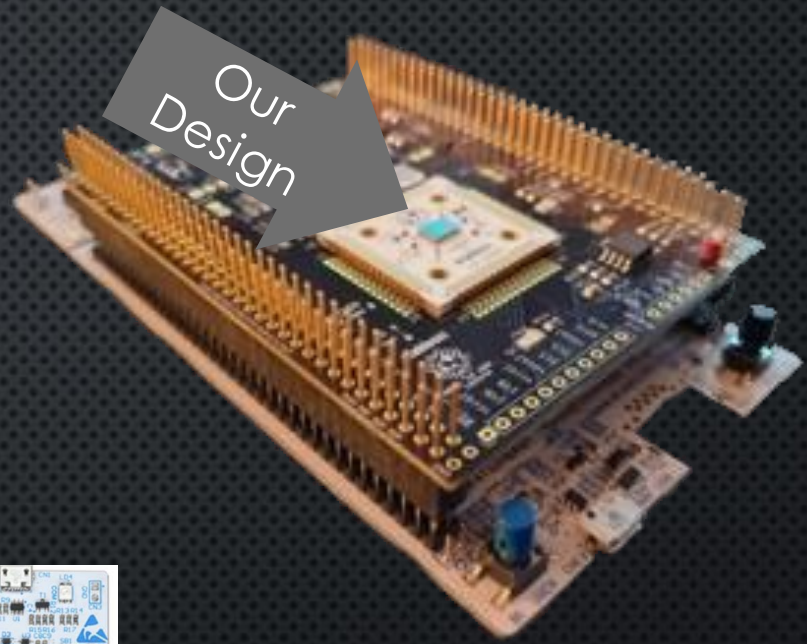
1. Background setup and assembly
2. Hardware Test
3. Software Test
4. SNN Chip Test
5. The test and simulation code

Physical Description

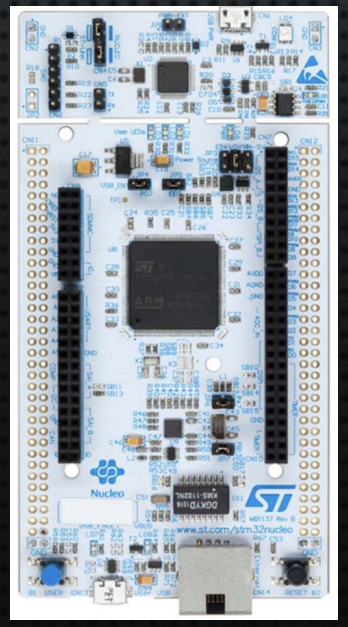
Caravel Nucleo Board
- Provides Interface

Caravel Nucleo Hat
- Mounting

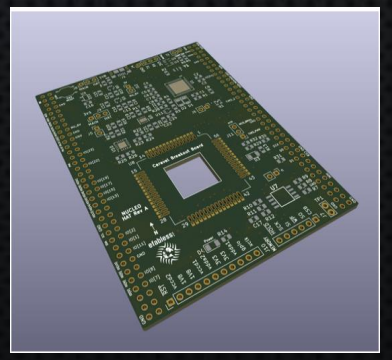
Caravel Breakout
- Holds Design



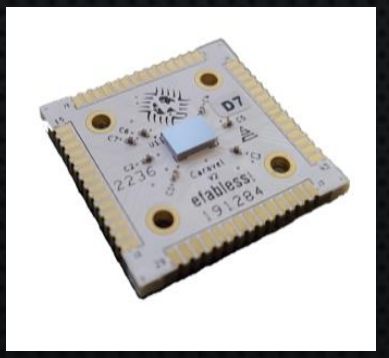
Efabless Caravel Board[6]



NUCLEO-F746ZG[5]



Caravel Nucleo Hat[6]



Caravel Breakout Boards with chip[6]

Goal 3 – Caravel Tutorial Document

Client Request:
Create a tutorial document to streamline the process of understanding all Open-Source tools for the chip design process.

Product to be Delivered:
Caravel Tutorial Document

Contents of Product:
1. 40 pages long.
2. Contains 8 sections of required information.
3. Contains 2 additional sections of supplementary information.

Tutorial Table of Contents ->


CONCLUSION

Challenges and Solutions

MPW Submission

MPW9 not yet open for submission and future of funding unclear

- Wait for next shuttle with project ready

Unclear / Outdated Information

Lots of conflicting information

- Asking questions in Slack, creating a document with all knowledge

Efabless program changes

Only 2 of 8 shuttles were returned with changes to the bring-up each time

- Efabless provides a lot of test and simulation code
- Ask question to Slack

Future Work

Next Steps:

Submission of our chip design to the next MPW Submission.
Bring up of our SNN chip design in the Caravel Infrastructure.

Improvements to be Made:

More in-depth analysis and testing of the Caravel Tutorial Document.

a. Only internal testing of the document has been performed

Performance Improvements for the SNN

a. Larger data-width for better precision and more accurate inferences
b. Minimize sources of BW bottlenecking to improve inference speed
c. Find ways to add more SRAM for higher resolution images

Conclusion

- Our project our goals:
  - Silicon prove a neuron model.
  - Create a bring up plan for our chip design.
  - Create a tutorial document for the Open-Source software tools used.
- We have accomplished all our objectives to a reasonable degree.
- Still further steps to take as well as improvements to be made.

Bibliography

[1] Yamazaki, K., Vo-Ho, V. K., Bulsara, D., & Le, N. (2022). Spiking Neural Networks and Their Applications: A Review. Brain sciences, 12(7), 863. https://doi.org/10.3390/brainsci12070863

[2] Erickson, B. J., Korfiatis, P., Akkus, Z., & Kline, T. L. (2017). Machine Learning for Medical Imaging. Radiographics : a review publication of the Radiological Society of North America, Inc, 37(2), 505–515. https://doi.org/10.1148/rg.2017160130

[3] Jason K. Eshraghian, Max Ward, Emre Neftci, Xinxin Wang, Gregor Lenz, Girish Dwivedi, Mohammed Bennamoun, Doo Seok Jeong, and Wei D. Lu "Training Spiking Neural Networks Using Lessons From Deep Learning". arXiv preprint arXiv:2109.12894, September 2021.

[4] *Hashlake Blockchain*, https://www.hashlake.io/?msclkid=75a76a1a43a21dd6d9dc0e5a16821f6c&utm_source=bing&utm_medium=cpc&utm_campaign=Web+search+2023&utm_term=asic+miner+values&utm_content=Asic+Miner

[5] STMicroelectronics.(2014). STM32 microcontrollers: UM1974 https://www.st.com/resource/en/user_manual/um1974-stm32-nucleo144-boards-mb1137-stmicroelectronics.pdf

[6] Efabless. (n.d.). *Efabless/caravel_board*. GitHub. Retrieved April 17, 2023, from https://github.com/efabless/caravel_board

SUPPLEMENTAL SLIDES

Data Path

Wishbone Feed

- Pixel values <- MNIST
- Weights <- pretrained snnTorch network
- Addresses <- CPU

Randomizer

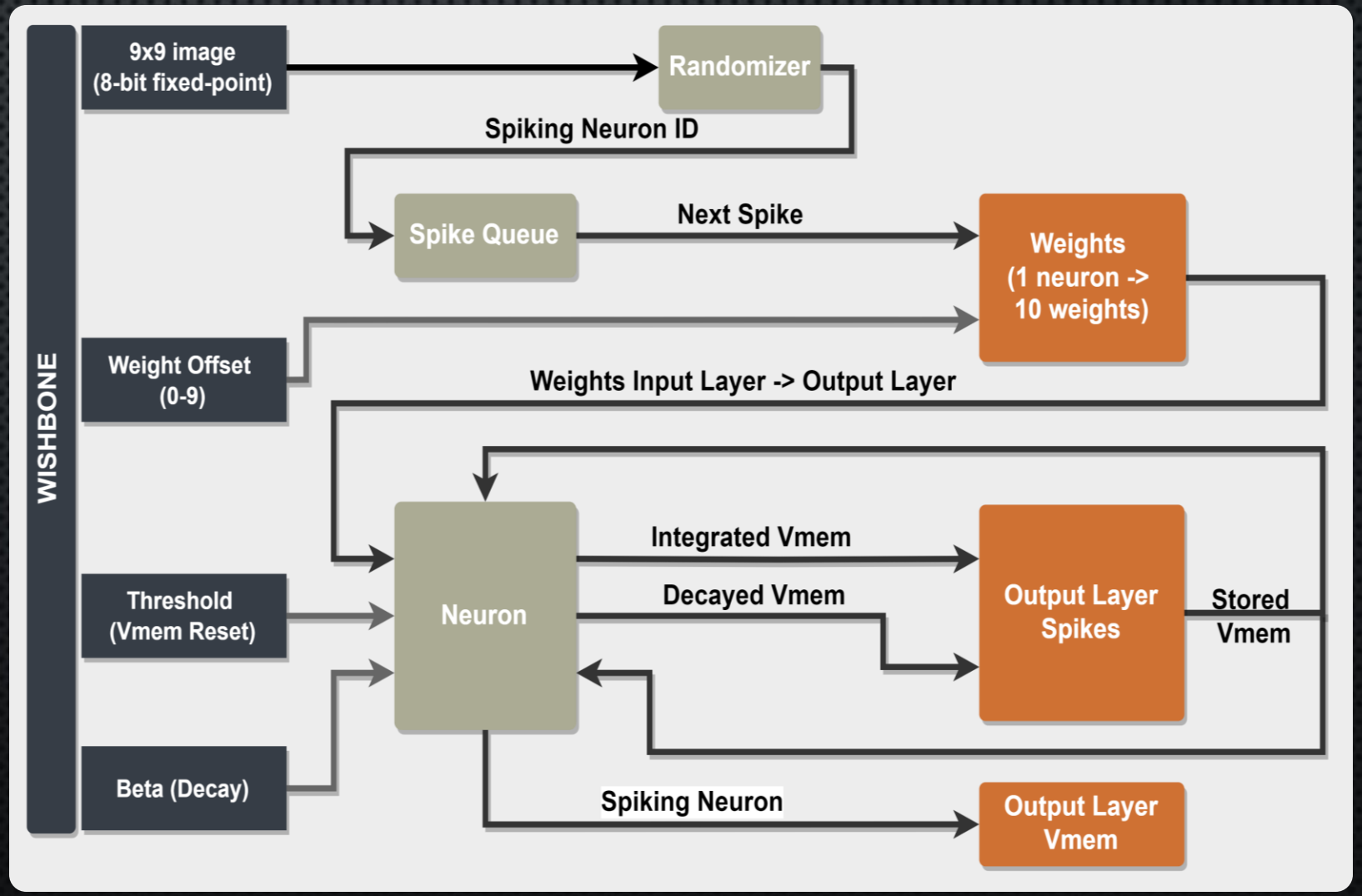
- Pseudo random no. generator
- Seed with image values

Spike Queue

- FIFO holder for Spikes

Neuron

- LIF hardware model



Goal 1 - Challenges and Solutions

MPW Submission

MPW9 not yet open for submission
Unclear future of funding
- Wait for next shuttle with project ready

Unclear / Outdated Information

Lots of conflicting information
Information exists in random Slack threads and outdated forums
- Asking questions in Slack, creating a document with all knowledge

Space

Minimal space creates memory constraints
- Reducing network size and data precision

Goal 2 - Challenges and Solutions

Efabless program changes

- Only 2 of 9 shuttles returned with changes to bring-up each time
- Efabless provides a lot of test and simulation code, but some of them have issues need to fix
- Ask question to Slack

Hard to try our program and debug the code

- Due to unavailable the physical board, it is hard for us to test our code and give expected output image.

Testing setup is complicated

- There are a lot of steps details, equipment and software tools we need to use. Easy to miss a step and need redo from the beginning.
- Make the bring up plan in more details.

Challenges and Solutions

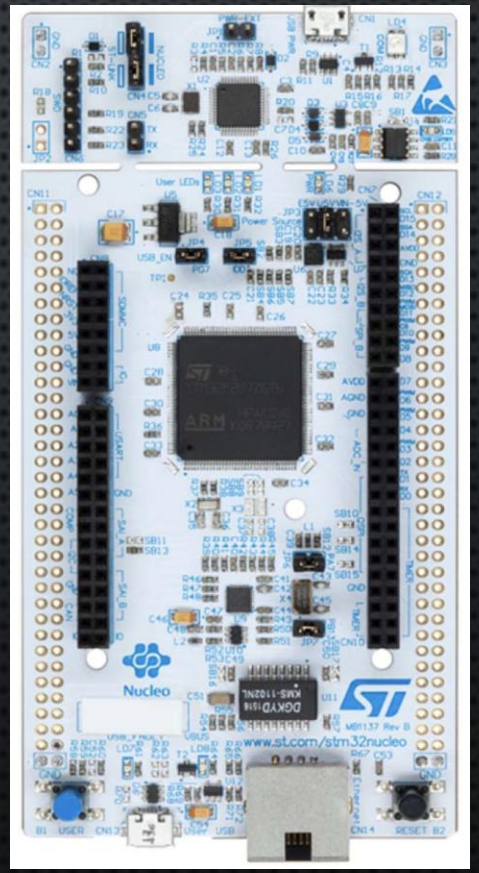
Limited documentation and conflicting/outdated information:

- Tested each documents information case by case.
- Communicated with Efabless personel through Slack
- Accumulated all the up-to-date info & links in the Caravel Tutorial Document.

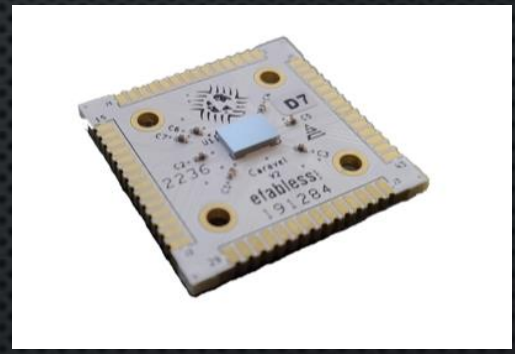
Physical Configuration

The components in our Efabless project:

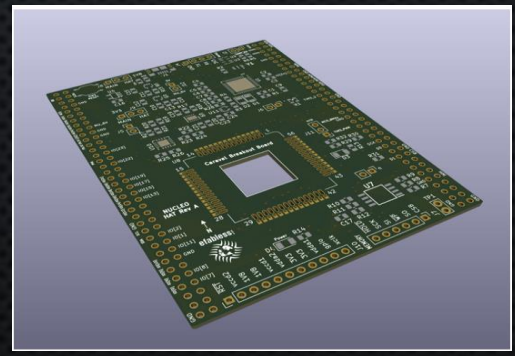
- NUCLEO-F746ZG or NUCLEO-F413ZH
- Caravel Nucleo Hat
- Caravel breakout boards with a Caravel part installed
- One or more chips (The SNN Chip we design)
- Two jumpers for J8 & J9
- USB micro-B to USB-A cable



NUCLEO-F746ZG[5]



Caravel Breakout Boards with chip[6]



Caravel Nucleo Hat[6]

Key Contributions

Katherine Gisi

Team Direction and Communication

- Worked at organizing tasks, people, agendas, and times
- Kept tabs on various components

Diagram Drawing and System Organization

- Created system, block, process, and data level drawings/diagrams
- Was a sounding board for design

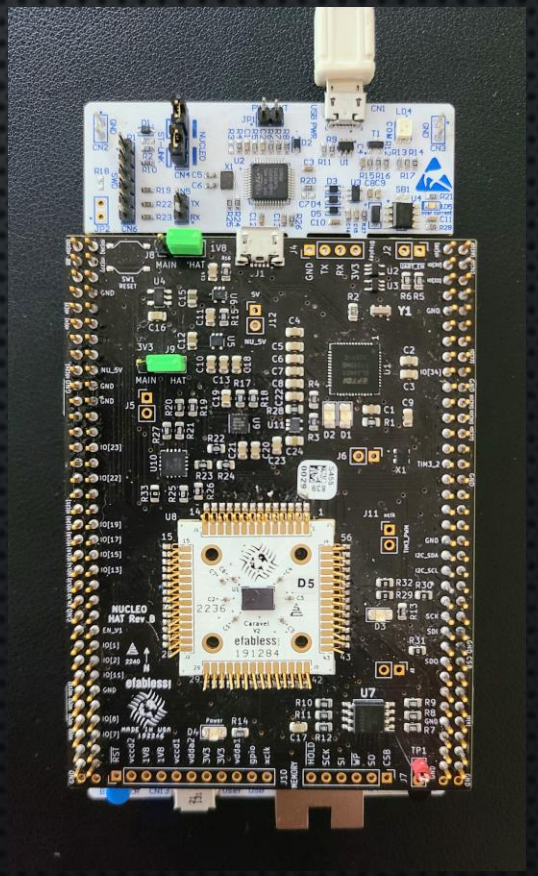
Research

- Kept up with Efabless updates on shuttle status and slack channel announcements
- Gained working understanding of SNNs, Digital Neurons, Test Benches, and ASIC flow

Key Contributions

Fulai Zhu

- PCB Research
  - provides an introduction and overview of the efabless caravel_board and caravel_Nucleo
  - Show all the components in the caravel_Nucleo and how each board connect
- Bring up Test Plan
  - Write the document about how to test our Efabless project
  - Hardware and software test plan and setting
  - Simulation setting

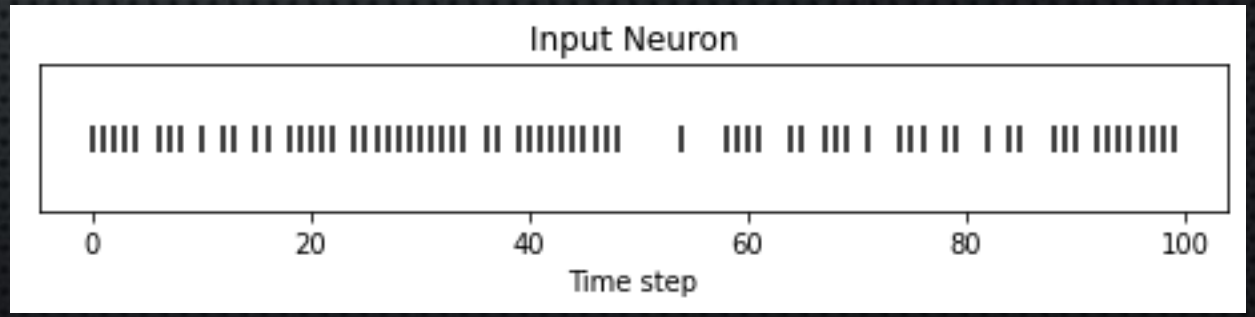


https://github.com/efabless/caravel_board/blob/main/firmware_vex/nucleo/docs/caravel+nucleo.jpg

Key Contributions

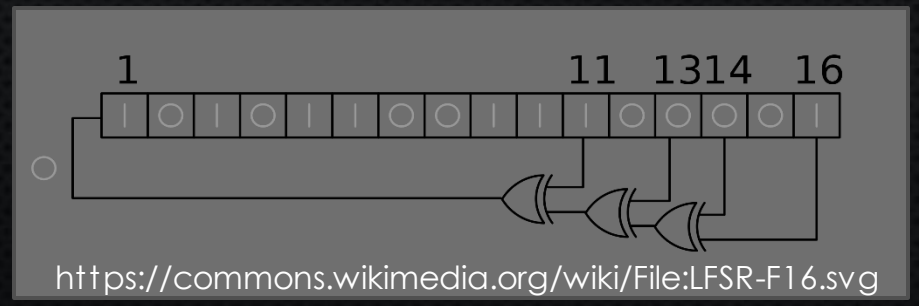
Tyler Green

- Tool Research and Documentation
  - Wishbone and Logic Analyzer
  - Interrupts
  - Simulation tools
- RTL implementation
  - SNN control logic
  - Spike queue
  - LFSR random number generator



https://snntorch.readthedocs.io/en/latest/tutorials/tutorial_1.html

https://github.com/gtkwave/gtkwave/blob/master/gtkwave3/share/icons/gtkwave_256x256x32.png

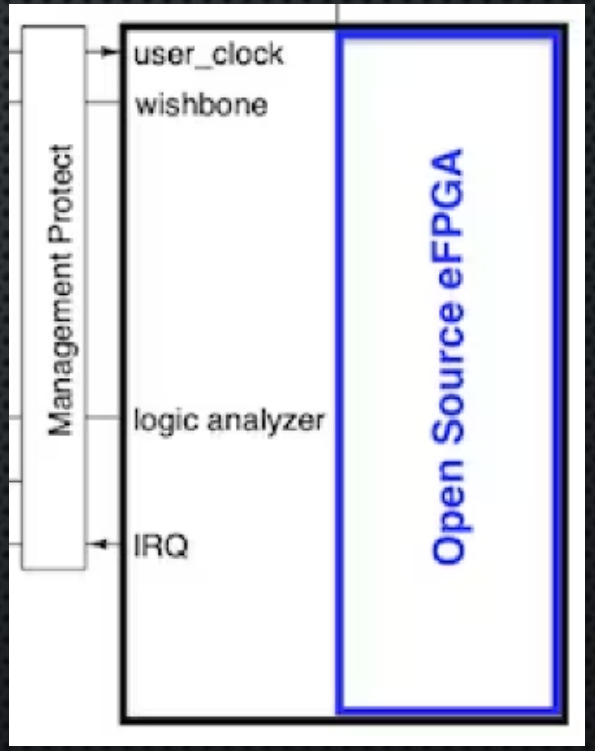


https://commons.wikimedia.org/wiki/File:LFSR-F16.svg

Key Contributions

William Zogg

- SNN Architecture Design
  - SNN Control Logic
  - Inter-module connections
- RTL Implementation
  - SNN Control Logic
  - Inter-module connections
- RTL Verification
  - SNN Control datapath
  - Wishbone data



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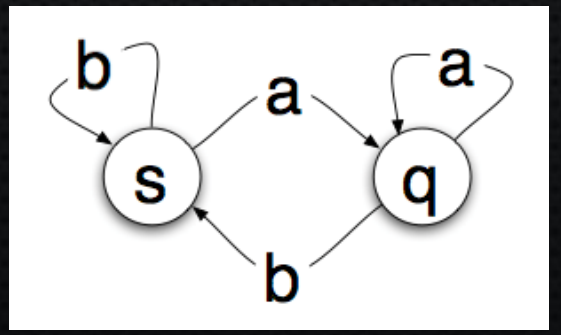

https://cdn-media-1.freecodecamp.org/images/0*msRB3BVpVkGVgEOd.

Key Contributions

Aaron Sledge

- Creation of the Caravel Tutorial Document
  - Over thirty pages in total
  - Created a majority of the sections in the document
  - Details how to acquire and how to use essential Efabless tools
  - Details how to acquire and use supplemental, but not essential, open-source software tools

Key Contributions

1. **William Zogg**
   SNN Architecture Design, RTL Implementation

2. **Tyler Green**
   Software Tool Research, Documentation, RTL Implementation

3. **Katherine Gisi**
   Team Direction/Communication, Diagram Drawing & System Organization, Research

4. **Aaron Sledge**
   Software Tool Research & Caravel Tutorial Document

5. **Fulai Zhu**
   PCB Research & Bring up Test Plan

IDEAS FOR INDUSTRY REVIEW PANEL PRESENTATION

- Maybe include a picture of our GIT repository
- Klayout view of our project design in the user area of the caravel harness
- Pictures of diagram along with the test bench results to demonstrate functionality of design
- Pictures of the integration of modules along with test bench results of the integration testing of the modules
- Pictures of overall system along with results of sending an image through it
  - Giff of how the neurons in our design should act, something simple and consumable that will be easily understood by those who don't quite understand chip design/neuron models
- Picture/quick video demonstrating the tutorial document
- Pictures of the PCB our chip would be returned on for mpw9
- Possibly include a picture of our bring up plan if we get around to it in time